ABSTRACT

The problems noted above are solved in large part by a computer system having one or more processors. Each processor has a branch predictor which dynamically predicts each conditional branch instruction. Software written for the processors to execute includes static branch prediction instructions embedded in the software. Each branch prediction instruction includes a pair of predictor bits that corresponds to another instruction which may be a conditional branch instruction. The pair of bits encodes whether, assuming the corresponding instruction is a branch, the branch is predicted as taken or not taken. This information encoded in the branch prediction instruction overrides the dynamic branch predictor in the processor. If the corresponding instruction is not a branch or a static prediction is not desired, the pair of bits is encoded to instruct the processor not to use static prediction for the corresponding instruction.

The processor also includes fetch logic which fetches instructions. The static branch prediction instruction identifies itself to the processor by including a predetermined register identifier that does not correspond to a register in the processor. The fetch unit examines the fetched instructions for that predetermined value to identify the static branch prediction instructions.